Amendments to the Claims

1. (CURRENTLY AMENDED) A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of individual shapes comprising:

a semiconductor substrate having an active area containing a channel region;

a floating Poly-Si gate with a bottom surface and a multiply connected top surface;

said bottom surface being flat and overlying said channel region in said active area;

said multiply connected top surface overlying said bottom surface and said channel region; said multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of said multiply connected top surface overlying said channel region in said active area is greater than the area of said bottom surface;

wherein said individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes;

said multiply connected top surface comprising more than three (3) ~~five (5)~~

individually connected top surfaces defined by said multiple regions of individual cross sectional shapes;

a conformal inter-poly dielectric layer replicating said individual cross-sectional shapes over said floating Poly-Si gate; and

a conformal Poly-Si control gate replicating said individual cross-sectional shapes over said inter-poly dielectric layer.

2. (ORIGINAL) A stacked-gate flash memory cell of claim 1, wherein said floating Poly-Si gate has a thickness between about 1900 to 2100 Å.

3. (PREVIOUSLY AMENDED) A stacked-gate flash memory cell having a floating Poly-Si gate with multiply connected surfaces of individual shapes comprising:

a semiconductor substrate having an active area;

a floating Poly-Si gate with a bottom surface and a multiply connected top surface;

said bottom surface being flat and overlying said active area;

said multiply connected top surface overlying said bottom surface; said multiply connected top surface being defined by multiple regions of individual cross-sectional shapes, wherein the area of said multiply connected top surface overlying said active area is greater than the area of said bottom surface;

wherein said individual cross-sectional shapes are selected from a group consisting of rectangular, trapezoidal and triangular shapes;

a conformal inter-poly dielectric layer replicating said individual cross-sectional shapes over said floating Poly-Si gate; and

a conformal Poly-Si control gate replicating said individual cross-sectional shapes over said inter-poly dielectric layer.

wherein said regions of individual cross-sectional shapes have a depth between about 900 to 1000 Å.

4. (CANCELLED)

5. (ORIGINAL) A stacked-gate flash memory cell of claim 1, wherein said inter-poly dielectric layer is oxide-nitride-oxide having a thickness between about 150 to 250 Å.

6. (ORIGINAL) A stacked-gate flash memory cell of claim 1, wherein said Poly-Si control gate has a thickness between about 1500 to 2000 Å.

Claims 7-20(cancelled).